

REMARKS

1. Claims 1-20 are pending in the application. Of these claims, claims 1-20 stand rejected and claims 10 and 13 are also objected to. This communication amends claims 1, 8, 10, 13 and 17; and cancels claims 7 and 16. Reconsideration of this application is respectfully requested.

2. Claims 10 and 13 stand objected to because the term "the chip" lacks an antecedent basis in the claim. In response, the term "the chip" recited in each of claims 10 and 13 has been amended to -- the substrate --. This term has a clear antecedent basis in claim 10. Accordingly, withdrawal of this objection is respectfully requested.

3. The Examiner contends that claims 10-19 are substantial duplicates of claims 1-9 and 20. In response, claim 1 has been amended to eliminate the limitation of "a conductive atomic force microscope."

4. Claims 1-7, 9-16 and 18-20 stand rejected under 35 USC 102(b) as being anticipated by U.S. Patent Publication 2003/0057988 to Maeda et al. (Maeda).

It is noted that Maeda has a publication date March 27, 2003, which is less than 1 year before Applicant's December 10, 2003 filing date. Accordingly, Maeda is not a reference under 35 USC 102(b).

Moreover, claim 1 has been amended to include the subject matter of canceled claim 7 and now recites "wherein the DC voltage applied to between the substrate and the tip of the probe during the voltage applying step is varied among at least two values, and the measuring step includes measuring the value of the tunneling current at each value of the applied DC voltage." Claim 10 has been amended to include essentially the subject matter of canceled claim 16 and now recites "wherein the DC voltage applied between the substrate and the tip of the probe in the voltage applying step is varied among at least two values, and for each of the contacts, the measuring step includes measuring the value of the tunneling current at each value of the applied DC voltage."

Maeda does not expressly or inherently describe, teach or suggest the subject matter of claims 1 and 10 because Maeda's method uses only a single bias voltage as

taught, for example, in paragraph [0029] "given forward bias voltage (e.g. 1.0 V) applied between the cantilever 3 and the semiconductor substrate 4."

In the claimed invention, graphs can be generated which plot the measured values of the tunneling current versus the corresponding values of the applied DC biasing voltages for the specified or suspected contacts (I/V curves). The graphs allow high resolution and high sensitivity current mapping of the semiconductor device contacts. The single voltage method of Maeda does not allow the semiconductor device contacts to be mapped with high resolution and sensitivity.

Therefore, Maeda does not anticipate claims 1 and 10. Claims 2-6, 9 and 20; and claims 11-15, 18 and 19 are not anticipated by Maeda for at least the same reasons as set forth with respect to claims 1 and 10 from which the claims in these groupings respectively depend.

In view of the foregoing, withdrawal of this rejection is respectfully requested.

4. Claims 8 and 17 stand rejected under 35 USC 103(a) as being unpatentable over Maeda in view of the document entitled "Introduction to VLSI Silicon Devices" by B. El-Kareh, page 93 (El-Kareh).

Claims 8 and 17 depend respectively from claims 1 and 10, and therefore, include the subject matter of these claims. As discussed above, Maeda fails to describe, teach or suggest the subject matter of claims 1 and 10.

El-Kareh merely presents and discusses a graph plotting the forward I-V characteristics of a pn junction. Such a graph does not cure the deficiencies of Maeda. Moreover, the Examiner has not provided any motivation for modifying Maeda to include the plotting of tunneling current values against applied voltage values.

In addition, it is respectfully submitted that such a plot would not be possible in Maeda, as the method of Maeda does utilize the voltage applying and current measuring steps of claims 1 and 10. Hence, one of ordinary skill in the art, at the time of invention, would not have been motivated to modify the method of Maeda to include a plotting step, as recited in claims 8 and 17.

In view of the foregoing, claims 8 and 17 are patentable over Maeda in view of El-Kareh. Accordingly, withdrawal of this rejection is respectfully requested.

5. Favorable reconsideration of this application is respectfully requested as it is believed that all outstanding issues have been addressed herein and, further, that claims 1-6, 8-15 and 17-20 are in condition for allowance, early notification of which is earnestly solicited. Should there be any questions or matters whose resolution may be advanced by a telephone call, the examiner is cordially invited to contact applicants' undersigned attorney at his number listed below.

6. No fees are due with this communication. The Commissioner is hereby authorized to charge payment of any additional filing fees required under 37 CFR 1.16 and any patent application processing fees under 37 CFR 1.17, which are associated with this communication, or credit any overpayment to Deposit Account No. 50-2061.

Respectfully submitted,



Paul A. Schwarz
Reg. No. 37,577

Duane Morris LLP
P.O. Box 5203
Princeton, NJ 08543-5203
609-631-2446- Tel
609-631-2401 - Fax